Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently amended) A memory device, comprising:

a first pair of fins comprising a first fin and a second fin formed substantially parallel to one another, the first fin and second fin having a first width and being located a distance from one another that is approximately twice the first width;

a second pair of fins comprising a third fin and a fourth fin formed substantially parallel to one another, the third fin and fourth fin having the first width and being located a distance from one another that is approximately twice the first width, wherein the second fin and the third fin are formed substantially parallel to one another and located a distance from one another that is approximately four times the first width;

~~a plurality of fins formed adjacent to one another, at least one of the fins being doped with a first type of impurities and at least one other one of the fins being doped with a second type of impurities;~~

a source region formed at one end of each of the fins;

a drain region formed at an opposite end of each of the fins;

a gate formed over the first fin and the second fin ~~two of the plurality of fins~~;

a wordline formed over each of the ~~plurality of~~ fins; and

a bitline contact formed adjacent at least one of the ~~plurality of~~ fins.

2. (Currently amended) The memory device of claim 1, wherein [[a]] the first width ~~of each of the fins~~ ranges from about 50 Å to about 500 Å.

3. (Original) The memory device of claim 1, wherein a height of each of the fins ranges from about 50 Å to about 500 Å.

4. (Canceled)

5. (Currently amended) The memory device of claim 1, wherein ~~a first pair of the plurality of~~ the first and third fins [[is]] are doped with a first type of impurities and the ~~second pair of the plurality of~~ second and fourth fins [[is]] are doped with a second type of impurities.

6. (Currently amended) The memory device of claim [[1]] 5, wherein the first type of impurities includes n-type impurities and the second type of impurities includes p-type impurities.

7-16. (Canceled)

17. (Currently amended) A method for forming a memory device, comprising:

forming a first fin and a second fin substantially parallel to one another and to each have a first width and to be located a distance from one another that is approximately twice the first width;

forming a third fin and a fourth fin substantially parallel to one another and to each have the first width and to be located a distance from one another that is approximately twice the first width and such that the second fin and the third fin are substantially parallel to one

another and located a distance from one another that is approximately four times the first width;

~~forming a plurality of fins adjacent to one another, at least one of the fins being doped with a first type of impurities and at least one other one of the fins being doped with a second type of impurities;~~

forming a source region at one end of each of the fins;

forming a drain region at an opposite end of each of the fins;

forming a gate over the first fin and the second fin ~~two of the plurality of fins~~;

forming a wordline over each of the ~~plurality of~~ fins; and

forming a bitline contact adjacent at least one of the ~~plurality of~~ fins.

18. (Original) The method of claim 17, wherein the memory device comprises a static random access memory (SRAM).

19. (Canceled)

20. (Canceled)

21. (New) The method of claim 17, wherein the first width ranges from about 50 Å to about 500 Å.

22. (New) The method of claim 17, further comprising:

performing a first tilt angle implant process to dope the first and third fins with a first

type of impurities; and

performing a second tilt angle implant process to dope the second and fourth fins with a second type of impurities.

23. (New) The method of claim 22, wherein the first type of impurities includes n-type impurities and the second type of impurities includes p-type impurities.

24. (New) A device, comprising:

a first fin and a second fin formed substantially parallel to one another and located approximately a distance *d* from one another;

a third fin and a fourth fin formed substantially parallel to one another and located approximately the distance *d* from one another, wherein the second fin is formed substantially parallel to the third fin and is located approximately twice the distance *d* from the third fin and wherein the first and third fins are doped with n-type impurities and the second and fourth fins are doped with p-type impurities;

a source region formed at one end of each of the first, second, third and fourth fins;

a drain region formed at an opposite end of each of the first, second, third and fourth fins; and

a gate formed over the first and second fins.

25. (New) The device of claim 24, further comprising:

a wordline formed over each of the first, second, third and fourth fins; and

a bitline contact formed adjacent at least one of the first, second, third and fourth fins.

26. (New) The device of claim 25, wherein the device comprises a static random access memory (SRAM).